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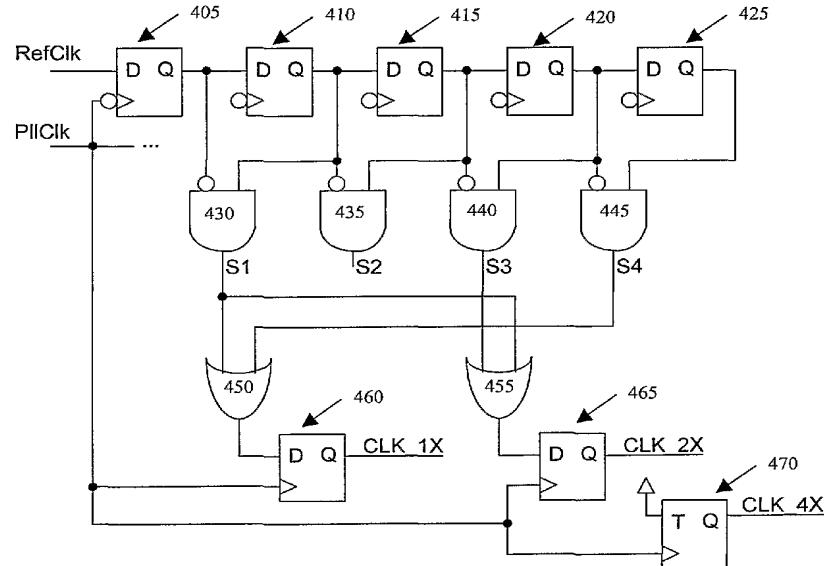
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(54) Title: ANALOG TO DIGITAL CONVERTER CLOCK SYNCHRONIZER



(57) Abstract: The present application generally relates to apparatuses such as television signal processing apparatus that process radio frequency signals. More specifically, the present application is particularly useful in integrated circuits that must receive a radio frequency signal and simultaneously use circuitry where the timing of the operations are based on the received RF signal and circuitry where the timing is based on a fixed rate signal with sensitivity to clock jitter. According to an exemplary embodiment, the apparatus comprises, a first input (RefClk), a second input (PllClk), an output (CLK 1X), a delay means (405, 410, 415, 420, 425), and a logic means (430, 435, 440, 445, 450, 455, 460, 465, and 470) to compare a plurality of stages of said delay means to produce an signal at said output.

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